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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/564,079	01/09/2006	Ernst Bretschneider	DE03 0241 US1	7528
65913	7590	12/11/2008	EXAMINER	
NXP, B.V. NXP INTELLECTUAL PROPERTY DEPARTMENT M/S41-SJ 1109 MCKAY DRIVE SAN JOSE, CA 95131			PARIHAR, SUCHIN	
			ART UNIT	PAPER NUMBER
			2825	
			NOTIFICATION DATE	DELIVERY MODE
			12/11/2008	ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

<b>Office Action Summary</b>	<b>Application No.</b> 10/564,079	<b>Applicant(s)</b> BRETSCHNEIDER, ERNST	
	<b>Examiner</b> SUCHIN PARIHAR	<b>Art Unit</b> 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 15 August 2008.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-6 and 8-14 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-6, 8, 9 and 11-13 is/are rejected.
- 7) ☒ Claim(s) 10 and 14 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

### DETAILED ACTION

1. This NON-FINAL office action is in response to application 10/564,079, amendment filed on 8/15/2008. Claim 7 is cancelled. Claims 1-6 and 8-14 are currently pending in this application.
2. Applicant's arguments filed on 8/15/2008 have been considered. A new ground(s) of rejection has been made.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. **Claims 1-6, 8-9 and 11-13 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Lippmann et al. (2003/0127709) in view of Kash et al. (US 2007/0030022).

5. With respect to claim 1, Lippmann teaches:

a security-sensitive (security critical ICs, paragraph [0006]) semiconductor product, particularly a smart-card chip (smartcard, paragraph [0006]), comprising electrically active structures (active devices, paragraph [0002]) envisaged by the chip design (internal structure of the semiconductor chip, paragraph [0004]) in the form of circuit functions (important functions of the chip, paragraph [0030]) in and on a wafer (each chip on the wafer, paragraph [0099]) and connected by electrical contacts (contacts, paragraph [0002]), and an additional, electrically conductive parts

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(electrically conductive polymer, paragraph [0012]), which are insulated from one another (insulator covering, paragraph [0029]), and wherein the parts of the filling structures that are generated are combined with the contacts (contacts that are separated and isolated from one another, paragraph [0002]).

Lippmann fails to explicitly teach:

additional circuit functions are generated in addition to the electrically active circuit structures that are produced for the circuit; and

wherein a majority of the fill structures generated are incorporated along a signal path so that active, electrically connected parts of the fill structures are situated next to dummy fill structures that are insulated from the active electrically connected parts of the fill structures.

However, Kash teaches:

additional circuit functions are generated as well as the circuit structures that are produced for the circuit (see addition of dummy circuit, Figure 17, also see paragraph [0070]); and

wherein a majority of the fill structures generated are incorporated along a signal path so that active, electrically connected parts (dummy circuit is in close proximity to actual circuit, see Figure 17, and paragraph [0070]) of the fill structures are situated next to (i.e. close proximity to, paragraph [0017]) dummy fill structures (dummy circuit is in close proximity to actual circuit, see Figure 17, and paragraph [0070]) that are insulated (insulation layer, opaque absorption structures covering circuits, paragraphs [0053]-[0056]) from the active electrically connected parts of the fill structures.

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It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Kash into the invention of Lippmann for at least the following reason: Kash improves the security enhancement of Lippmann (security-critical IC's, see Lippmann, paragraph [0006]) by providing a technique to further frustrate attempts to reverse engineer an IC such as to add additional circuits such as dummy circuitry to prevent reverse engineering which is a desirable achievement in the art (see Kash, paragraph [0054]).

6. With respect to claim 2, Lippmann teaches:

characterized in that the parts of the filling structures (filling the clearance with material, see Lippmann, claim 35) that are generated are composed of metal, of polycrystalline silicon (polysilicon, paragraph [0040]), of diffusion regions, or of other electrically conductive materials of the semiconductor product (semiconductor device, paragraph [0002]).

7. With respect to claim 3, Lippmann teaches:

characterized in that the contacts are also set by a routing program belonging to a design program for chip design (provided for the wiring, paragraph [0036]).

8. With respect to claim 4, Lippmann teaches:

characterized in that the passive fill structures composed of metal are connected together electrically, so that at least one closed signal path is formed between two or more nodes of the active circuitry of the circuit (plated-through paths to be established by vertical electrically conducting connections, paragraph [0066]).

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9. With respect to claim 5, Lippmann teaches:

characterized in that the contacts are set in such a way that arbitrary interlinkings, both horizontal and vertical, of the parts of the fill structure are produced (see Lippmann, figures 6 and 7).

10. With respect to claim 6, Lippmann teaches:

characterized in that the contacts are set in such a way that after each part of the fill structure the wiring level is changed and the horizontal direction is changed within the level (contacts that are separated and isolated from one another by intermetal dielectrics, paragraph [0002]).

11. With respect to claim 8, Lippmann teaches:

characterized in that the signal path is connected to further suitable integrated electronic circuit components such as, for example, transistors, diodes, resistors and capacitors (multi-layered resistance network, paragraph [0009]; transistor function, see Abstract).

12. With respect to claim 9, Lippmann teaches:

characterized in that the signal path that is composed of parts of the fill structures that are interlinked with one another is used as a supply track by connecting electronic circuit components to the supply voltage via the parts of the fill structures that are interlinked with one another (multi-layered resistance network, paragraph [0009]; transistor function, see Abstract).

13. With respect to claim 11, Lippmann teaches:

characterized in that a pick-off, which may be fed to electronic analyzer

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circuits, takes place between two contacts at a time on the signal path (contacts pick off a Hall voltage, paragraph [0017]).

14. With respect to claim 12, Lippmann teaches:

characterized in that the signal path that is composed of parts of the fill structures that are interlinked with one another is used as a resistive signal path, in which case the parts of the fill structures that are interlinked with one another are connected between the supply voltage and the ground potential of the electronic circuitry and, as well as this, semiconductor resistors are inserted in this path at random intervals by means of contacts that are set (multi-layered resistance network, paragraph [0009]; transistor function, see Abstract).

15. With respect to claim 13, Lippmann teaches:

characterized in that a pick-off, which may be fed to electronic analyzer circuits, takes place between two resistors at a time (contacts pick off a Hall voltage, paragraph [0017]).

***Allowable Subject Matter***

16. Claims 10 and 14 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten as described below and in independent form including all of the limitations of the base claim and any intervening claims.

17. With respect to claim 10, the prior art of record fails to explicitly teach:

wherein the signal path that is composed of parts of the fill structures that are interlinked with one another is used as a supply-to-ground path by causing the parts of the fill structures that are interlinked with one another to form an electrically conductive

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current path between the supply voltage and the ground potential of the electronic circuitry.

18. With respect to claim 14, the prior art of record fails to explicitly teach:

security means for impeding optical tracing of the electronic circuitry-sensitive semiconductor product by varying the sizes **and** positions of the interlinked parts of the fill structures.

### ***Response to Arguments***

19. Applicant's arguments have been considered. However, a new ground(s) of rejection has been made as detailed in the above rejections.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SUCHIN PARIHAR whose telephone number is (571)272-6210. The examiner can normally be reached on Mon-Fri, 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business



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Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Paul Dinh/  
Primary Examiner, Art Unit 2825

/Suchin Parihar/  
Examiner, Art Unit 2825